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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/737,218	12/14/2000	Robert D. Norman	703.070US2	1359

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EXAMINER	
PEIKARI, BEHZAD	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,218	NORMAN ET AL.	
	Examiner	Art Unit	
	B. James Peikari	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 64-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 64-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 26, 2003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 64-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al., U.S. 5,617,537.

Yamada et al. teach the present invention with a memory system comprising: A plurality of memory devices (*21, e.g., 21-1, 21-2 and 21-3*) associated with one processor (*note that each of the memory devices 21-1, 21-2 and 21-3 is associated with any one of the processors 19-1, 19-2 and 19-3 and any one processor may access all of*

these memory devices via processor interconnect 25), with each memory device comprising:

(a) an array of memory cells (*each memory 21 is made up of memory cells*);

(b) an addressing circuitry operatively coupled to the array of the memory cells, wherein the addressing circuitry is capable of providing addresses to the array of memory cells (*note "The distributed shared memories are assigned global addresses common to all processor modules", in the abstract and the "object ID" used throughout – "the destination of a message is specified by the object ID"*);

(c) a memory device bus interface (*there are several for each device 21 – one to interface with the system bus, namely coupler 22, and one to interface with the multiprocessor communication lines, namely adaptor 24, and one to provide protection from either route, namely protector 23*);

(d) a command decoder which decodes commands at the memory device bus interface (), including an address assign command (*30*); and

(e) a local address storage circuitry which stores a local address for identifying the storage circuitry's single associated memory device once the address assign command is decoded by the command decoder (*the local address, as well as the addresses of other devices, is stored in each PM in map area 21M*); and

(f) a memory controller having a controller bus interface coupled to the memory device bus interface, with the memory controller providing the local address to be stored in the local address storage circuitry of the memory device of the memory system together with the address assign command (*see below*).

As for the claimed use of a system bus for performing the functions above, as in claims 2 and 3, the processor interconnect 25 "can be implemented as a system bus" (note column 7, lines 10-13).

Yamada et al. teach the function of the invention as presently claimed, but fail to specifically mention the act of assigning the addresses to the memories (in other words, each of the memories have been assigned addresses, as in the invention, but Yamada et al. do not disclose the specifics of how the address were put there).

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a memory controller (with a requisite interface) in order to assign addresses to each of the units in Yamada et al., since (1) the addresses were assigned to each memory and something had to put them there, (2) there was no way that the addresses could have been pre-assigned at manufacture -- there must have been some control circuitry to assign address dynamically, since the Yamada et al. PMs were designed to be part of the type of large multiprocessor systems (which are constantly being reconfigured as units are added or deleted), (3) the memory control circuitry would have had to be sophisticated enough to provide *unique* global addresses for each object in the network and (4) the dynamic address assignment would have been critical to speeding up message passing (the need for speed was clearly emphasized by the use of asynchronous message passing in Yamada et al.)

As stated in the rejection, each memory device 21-1, 21-2 and 21-3 may be associated with any one processor, e.g., processor 19-1, to the extent that the processor 19-1 actually has access to data from each memory device via line 30-1 and

processor interconnect 25. However, Yamada et al. fails to specifically mention that a plurality of memory devices are associated with *only* one processor. However, upon review of the disclosure of the Yamada et al. system, it would have been obvious to one of ordinary skill in the art at the time of the invention to associate each memory device 21-1, 21-2 and 21-3 with only one processor, e.g. processor 19-1, since the structure is such that if processors 19-2 and 19-3 failed and/or had to be disconnected from system 17 for any reason, processor 19-1 would still have had unrestricted access to each memory device 21-1, 21-2 and 21-3 because interconnect 25 connected the processor 19-1 to the modules 18-2 and 18-3 containing memories 21-2 and 21-3, respectively, as opposed to a direct processor-to-processor interconnect. For example, if processor 19-1 had to communicate through processor 19-2 to access memory 21-2, then the connection between processor 19-1 and memory 21-2 would have been severed upon the failure and/or removal of processor 19-2. However, system 17 was set up to allow processor 19-1 access to memories 21-2 and 21-3 without having to go through processors 19-2 or 19-3. In fact, this efficient method of data transfer was taught as prior art by Yamada et al. (note Figure 1).

As for claim 74, this would have been taught by two systems 17.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-

3824. The examiner is generally available on alternate weekdays from 8:00 am to 9:00 pm, EST, and on weekends.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

B. James Peikari
Primary Examiner
Art Unit 2186

May 31, 2004